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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,748	12/19/2001	Yao Wen Chang	JCLA7648	9132

7590 10/07/2003

J.C. Patents, Inc.
4 Venture, Suite 250
Irvine, CA 92618

EXAMINER	
TRINH, HOA B	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,748	CHANG ET AL.	
	Examiner	Art Unit	
	Vikki H Trinh	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al. (6,441,434) in view of Yeh (6,133,055).

Long et al. '434 discloses a substrate 12; a gate 44 on the substrate; a gate dielectric layer 50 between the tortuous gate line and the substrate; and a source region 20 and a drain region 22 in the substrate beside the tortuous gate line, wherein the source region 20 has a broader part 32 and a narrower part 30, and the drain region 22 has a broader part 36 and a narrower part 34, wherein the broader part 32 of the source region is disposed opposite to the narrower part 34 of the drain region and the narrower part 30 of the source region is disposed opposite to the broader part 36 of the drain region. Fig. 2.

However, Long et al. does not explicitly teach that the gate is a tortuous gate. (The examiner interprets the phrase "tortuous gate" is to mean a non-linear gate).

Yeh discloses an IC device having a non-linear gate 70, 80. See figures 6-7.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the gate structure of Long et al. with a non-linear gate structure, as taught by Yeh, so as to easily measure defect and parasitic device effect. (See Yeh, col. 2, lines 60-65.)

As to claim 2, wherein at least a contact 54 is disposed on the broader part of the source region and at least a contact 56 is disposed on a broader part of the drain region. Fig. 2.

As to claim 3, wherein the material of the tortuous gate line comprises doped polysilicon. Col. 6, line 23.

As to claim 4, a substrate12 ; a gate 44 on the substrate; a gate dielectric layer 50 between the tortuous gate and the substrate, a source region 20 and a drain region 22 disposed within the substrate adjacent to the tortuous gate, wherein the source region has a broader part 32 and a narrower part 30, and the drain region has a broader part 36 and a narrower part 34, wherein the broader part 32 of the source region is disposed opposite to the narrower part 34 of the drain

region, and the narrower part 30 of the source region is disposed opposite to the broader part 36 of the drain region; and a metal-silicide layer 46 (col. 5, line2) disposed on the tortuous gate and on the source and drain regions. See figure 2.

However, Long et al. does not explicitly teach that the gate is a tortuous gate. (The examiner interprets the phrase "tortuous gate" is to mean a non-linear gate).

Yeh discloses an IC device having a non-linear gate 70, 80. See figures 6-7.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the gate structure of Long et al. with a non-linear gate structure, as taught by Yeh, so as to easily measure defect and parasitic device effect. (See Yeh, col. 2, lines 60-65.)

As to claim 5, wherein at least a contact 54 is disposed on the broader part of the source region and at least a contact is disposed on a broader part of the drain region. Fig. 2.

As to claim 6, wherein the material of the tortuous gate line comprises doped polysilicon. Col. 6, line 23.

As to claim 7, wherein the material of the metal-silicide layer is selected from the group comprising titanium silicide, cobalt silicide, nickel silicide, and palladium silicide. See col. 7, lines 45-48.

As to claims 8, 17, a substrate 12; a gate 44 on the substrate; a gate dielectric layer 50; a lightly doped source region 30, a source region 20, a lightly doped drain region 34, and a drain region 22 disposed within the substrate located adjacent to the tortuous gate line, wherein the lightly doped source region, the source region, the lightly doped drain region, and the drain region have a broader part and a narrower part, respectively, wherein the broader part 32 of the lightly doped source region / source region is opposite to the narrower part 34 of the lightly

doped drain region / drain region, and the narrower part 30 of the lightly doped source region / source region is opposite to the broader part 36 of the lightly doped drain region / drain region; and a metal silicide layer 46 disposed on the tortuous gate and a second metal silicide layer 54, 56 disposed on the source and drain regions. Fig. 2.

However, Long et al. does not explicitly teach that the gate is a tortuous gate. (The examiner interprets the phrase "tortuous gate" is to mean a non-linear gate).

Yeh discloses an IC device having a non-linear gate 70, 80. See figures 6-7.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the gate structure of Long et al. with a non-linear gate structure, as taught by Yeh, so as to easily measure defect and parasitic device effect. (See Yeh, col. 2, lines 60-65.)

As to claims 9, 18, wherein at least a contact 54 is disposed on the broader part of the source region and at least a contact is disposed on a broader part of the drain region. Fig. 2.

As to claims 10, 19, wherein the material of the gate comprises doped polysilicon. Col. 6, line 23.

As to claim 11, wherein the material of the first metal-silicide layer is selected from one of the group comprising titanium silicide, cobalt silicide, nickel silicide. Col. 7, lines 45-48.

As to claim 12, wherein the material of the second metal-silicide layer is selected from one of the group comprising titanium silicide, cobalt silicide, nickel silicide. Col. 7, lines 45-48.

As to claim 13, wherein the material of the first metal-silicide layer 46 on the tortuous gate and the material of the second metal silicide layer 54/56 of the source/drain regions are substantially of same material. Col. 7, lines 45-48.

As to claim 14, wherein the material of the first metal-silicide layer 46 on the tortuous gate is different from that of the second metal-silicide layer 54/56 on the source/drain region. Col. 7, lines 45-48.

As to claim 15, wherein the material of the first metal-silicide layer is titanium silicide. Col. 7, lines 45-48.

As to claim 16, wherein the material of the second metal-silicide layer on the source/drain region is titanium silicide. Col. 7, lines 45-48.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
   Jiang et al. (5,925,914) discloses a MOSFET with asymmetric s/d structure.

2. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (703) 308-8238. The Examiner can normally be reached Mon-Tuesday, Thurs-Friday, 7:30 AM - 6:00 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (703) 308-4918. General inquiries relating to the status of this application should be directed to the Group receptionist at (703) 308-0858. The fax number is (703) 308-2708.

Vikki Trinh,
Patent Examiner
AU 2814

SU